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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,148	06/29/2000	Takehiko Tsuchiya	03180.0255	7735

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EXAMINER	
CHANG, SUNRAY	

ART UNIT	PAPER NUMBER
2121	7

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,148	TSUCHIYA ET AL.	
	Examiner	Art Unit	
	Sunray Chang	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2000*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. *This office action is in responsive to the paper 6 filed on April 5th, 2004*

2. *Claims 1 – 16 are presented for examination.*

Claims 1 – 16 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilbert et al. (U.S. Patent No. 5,805,861, and referred to as Gilbert hereinafter).

4. Regarding independent claims 1, 3, and 8, Gilbert teaches a logic verification unit (50, Fig. 4) configured to perform a logic verification (50, Fig. 4) by using a circuit description (new, old design version, 42 – 44, Fig. 4) defining a structure and a specification of a circuit (design version, 42 – 44, Fig. 4) to be designed and a plurality of test vectors (names, 54 – 60, Fig. 4); a profile information generating unit (42 – 44, Fig. 4) configured to store information (database, 42 – 44, Fig. 4) about a plurality of logic cones (cone of logic, 48, Fig. 4) in the circuit description (design version, 48, Fig.

4) to be activated by the test vectors (select cone of logic from both design version, 48, Fig. 4) during the logic verification (50, Fig. 4) in every test vector (names, Fig. 50) as a profile information (design version, 42 – 46, Fig. 4); a logic cone specifying unit (48, Fig. 4) configured to specify (select, 48, Fig. 4) changed logic cones (cone of logic, 48, Fig. 4) of a changed circuit description (new design version, 44, Fig. 4) automatically (Fig. 4); and a test vector classifying unit (54, 58, Fig. 4) configured to classify (transfer, 54, 58, Fig. 4) the test vectors (Names, 54 – 60, Fig. 4) into test vectors related to the changed logic cones (new logic, 60, Fig. 4) and test vectors (Names, 54 – 60, Fig. 4) unrelated to (unchanged, 58, Fig. 4) the changed logic cones (new design version, by using the profile information (design, 42 – 46, Fig. 4).

5. Regarding dependent claims 2, 4, and 11, Gilbert teaches a logic cone dividing unit (46, Fig. 4) configured to divide (46, Fig. 4) the circuit description (design version, 46, Fig. 4) into the logic cones (cones of logic, 46, Fig. 4); circuit changing unit for changing (changed, Col 4, Line 5) first circuit description (integrated circuit, Col 4, Line 5) and generating (operated, Col 4, Line 5) a second circuit description (current design iteration, Col 4, Line 6); formal verification unit for verifying (verified, Col 7, Line 9) by formal technology (desired specification, Col 7, Line 10) using first and second circuit descriptions (behavior, detailed description, Col 7, Line 10 – 12);

6. Regarding dependent claims 5, 9 and 12, Gilbert teaches logic verification (identical logical structure, Col 5, Line 5) of the changed circuit description (current

circuit design, Col 5, Line 7) is executed (transferred, Col 5, Line 7) by using preferentially the test vectors (new components and net names, Col 5, Line 8) relating to (corresponding sections, Col. 5, Line 5) the changed logic cones (selected cone of logic design, Col. 5, Line 6).

7. Regarding dependent claims 6 and 10, Gilbert teaches issuing conversion process, Col 7, Line 13) a circuit description (detailed description, Col 7, Line 14) and processing (complete, Col 7, Line 20) circuit manufacture (layout, Col 7, Line 22) by using the circuit description (detailed description, Col 7, Line 18).

8. Regarding dependent claim 7, Gilbert teaches issuing (conversion process, Col 7, Line 13) a circuit description (detailed description, Col 7, Line 14) and processing circuit design (remaining design processes, Col 7, Line 17) and manufacture (layout, Col 7, Line 22) by using the circuit description (detailed description, Col 7, Line 14).

9. Regarding dependent claims 13, 15 and 16,

- **second and subsequent** logic **verifications** are executed by using **only the test vectors** relating to the **changed logic cones**.

  Gilbert teaches incremental design changes (**changed logic cones**) do not result (**only**) in unnecessary modifications to placement and routing information because of name changes (**test vectors**). Therefore, large amounts of time are saved in the design and test cycle (**second and subsequent logic**

verifications) for integrated circuits because the result of previous design (unchanged parts) can be reused. (Col. 17, Line 33 – 39)

10. Regarding dependent claim 14,

- The **logic cone specifying unit** specifies the **changed logic cones** on the basis of **a result** of the **formal verification**.

  Gilbert teaches **logic cone specifying unit** (48, Fig. 4) specifies the **changed logic cones** (cone of logic from new design, 48, Fig. 4).

  Gilbert further teaches errors (**a result**) may be detected during the simulation and testing phases (**formal verification**) of the design cycle and then fixed (**changed**) in the behavioral description (**logic cones**). (Col. 2, Line 38 – 40)

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tokunoh et al. (U.S. Patent No. 5,892,678) discloses an input unit, a storage unit, a selecting unit, a decision unit, a process unit, a component entry unit, a verification unit, a circuit changing unit. Carpenter et al. (U.S. Patent No. 5,862,149) discloses identify fault present, circuit node, test vector, test pattern, cones of logic, logic design, automatically generating test patterns, verify, storage. Tsuchiya et al. (U.S. Patent No. 6,449,750) discloses test vector classification, logic verification, formal verification, circuit changing, specifying unit, storing, dividing. Johannsen et al.

(U.S. Patent No. 5,910,898) discloses circuit design tool, verify, logic equation, logical behavior.

Response to Amendment

Drawings

12. The amendment overcomes objections to figure 1, 2, 4A, 4B, 5A, and 5B by correcting the term "CORN" to "CONE", replacing the term "Divide Logic Corn" with "Divide Circuit Description into Logic Cones", and replacing the term "Predetermined unit" with "Logic Cone" in claims 1 – 11. Examiner has withdrawn the objection to drawings.

Claim Objections

13. The amendment overcomes objections for claims 1 – 4 and 8. Examiner has withdrawn the claim objections for claims 1 – 4 and 8.

Double Patenting

14. After consideration of the remarks to the Office Action, examiner has withdrawn the Double Patenting Rejection.

Claim Rejections - 35 USC § 112

15. The amendment overcomes the 35 U.S.C. 112, first and second paragraph rejections. The examiner has withdrawn the rejections under 35 U.S.C. 112, first and second paragraph to claims 1 – 11.

Claim Rejections - 35 USC § 102

16. Applicants' argument regarding lack of anticipation is agreed with. Kucukcakar does not disclose a logic verification unit, a profile information generating unit, a logic cone specifying unit, or a test vector classifying unit. However, Kucukcakar was not replied upon in the first office action for these features. The reference of Gilbert shows these features as stated above.

17. Applicants' argument for claim 2 is noted but is not agreed with. Applicants argue that, Gilbert fails to disclose the elements (storing information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information... and classifying the test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones by using the profile information.) As set forth in the rejection above, Gilbert discloses these features. Therefore, claim3 is not patentable and claim 8, since it is similar to claim 3, is also not patentable. Applicants have not separately argued claims 4 – 7 and 9 – 11 and thus these claims are also not considered to be patentable.

New claims 12 – 16 are rejected as set forth above.

Conclusion

18. THIS ACTION IS MADE FINAL. Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE – MONTHS from the mailing date of this action. In the event a first reply is filed within TWO – MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE – MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX – MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is (703) 305-8744. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (703)308-3179. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 746-3506.

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Technology Center 2100
U.S. Patent and Trademark Office

June 25, 2004